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| 10/821,872 | 04/12/2004 | Katsuhiro Uesugi | 67161-148 | 1856 |

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| EXAMINER | |
|---|---|
| KRAIG, WILLIAM F | |

| ART UNIT | PAPER NUMBER |
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| 2815 | |

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/821,872 | Applicant(s) UESUGI ET AL. | |
|---|---|---|---|
| | Examiner William Kraig | Art Unit 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10/21/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *1 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim 1 objected to because of the following informalities: There is an extraneous punctuation mark on the last line of the claim. Examiner recommends removing the period that appears after the word "and". Appropriate correction is required.

2. Claim 7 objected to because of the following informalities: There is an error on the line 3 of the claim. Examiner recommends replacing "sid" with --side--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 rejected under 35 U.S.C. 103(a) as being unpatentable over Bost et al. (US Patent 5270256) in view of Dinkel et al. (U.S. Patent 5834829).

Regarding claim 1, Figs. 18 and 19 of Bost et al., shown below, disclose a semiconductor device comprising:

a semiconductor substrate (30) having a main surface (30a, 170);

a semiconductor element (located within region 45)(Bost et al., Col.5, Lines 5-8), having side surfaces (defined by the edges of rectangle defining semiconductor element region (45)), formed on said main surface (30a, 170);

an interlayer insulating film (70,110) having a top surface (110a) and a peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), below) extending from said top surface (110a) to said main surface (30a, 170), and formed on said main surface (30a, 170) to cover (Bost et al., Col.5, Lines 12-15) said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)), wherein in said interlayer insulating film (70,110), a strip-like groove portion (191) is formed between a first side surface (one side of rectangle defining semiconductor element region (45)) of said semiconductor element (located within region 45)(Bost et al., Col 5, Lines 5-8)) and said peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1(a combined view of Figs. 18 and 19 of Bost et al., showing an angled view of a corner of the die (40) shown in Fig. 19, and the cross section of the die shown in Fig. 18) (drawn by the examiner), below), to extend in parallel with said main surface (30a, 170) and to extend in a predetermined direction; and

a metal (171) filling said groove portion (191).

Bost et al., however, fails to disclose there being two separately spaced apart strip-like second groove portion being formed between a first side surface of said semiconductor element and said peripheral edge, extending in a predetermined direction. Bost et al. also fails to disclose a plurality of third groove portions formed,

between the first side surfaces of said semiconductor element and said peripheral edge, to diverge from said first and second groove portions and to extend in a direction different from an extending direction of said first and second groove portions; and a metal filling said second and third groove portions.

Fig. 1 of Dinkel et al. teaches a similar semiconductor device wherein there are first (12) and second (14) separately spaced apart strip-like groove portions formed between a first side surface of a semiconductor element (side surface of active area (18))(Dinkel et al., Col. 2, Lines 25-36) and a peripheral edge of an insulating layer (Dinkel et al. describes an insulating layer covering the active area (18) in which the strip-like groove portions are formed (Dinkel et al., Col.2, Lines 31-36, 37-44, and 64-66)). Fig. 3A of Dinkel et al. further teaches a plurality of third groove portions (34, 36) formed, between the first side surfaces (side surface of active area (18))(Dinkel et al., Col. 2, Lines 25-36) of said semiconductor element and said peripheral edge (edge of insulating layer which Dinkel et al. describes as covering the active area (18) and in which the strip-like groove portions (30, 32) are formed (Dinkel et al., Col.2, Lines 31-36, 37-44, and 64-66))), to diverge from said first (30) and second (32) groove portions and to extend in a direction different from an extending direction of said first and second groove portions (In Fig. 3A of Dinkel et al. the directions in which the third groove portions (34, 36) extend can be seen to be different than the directions in which first and second groove portions (30, 32) extend); and a metal filling said second and third groove portions (Dinkel et al., Col. 2, Lines 40-44).

It would have been obvious to one of ordinary skill in the art to incorporate the second and third strip-like groove portions of Dinkel et al. into the device of Bost et al. The ordinary artisan would have been motivated to modify Bost et al. in the above manner for the purpose of providing a redundancy that is helpful in preventing crack propagation into the semiconductor active areas (Dinkel et al., Col. 3, Lines 33-34), and also to increase the amount of surface area by which the crack-propagating energy may be absorbed (Dinkel et al., Col. 3, Lines 58-62).

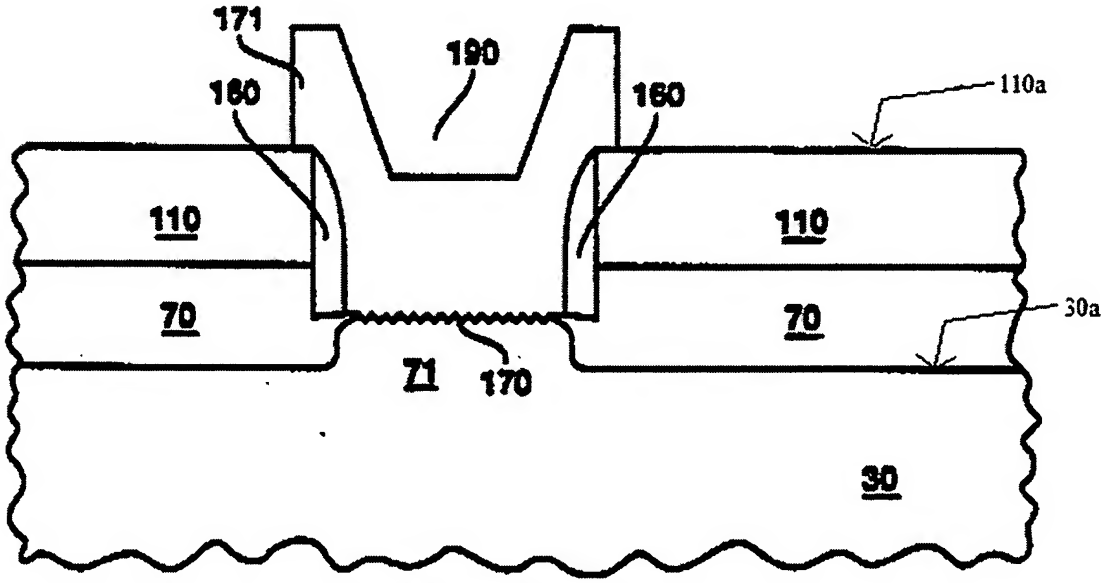


**FIGURE 18**

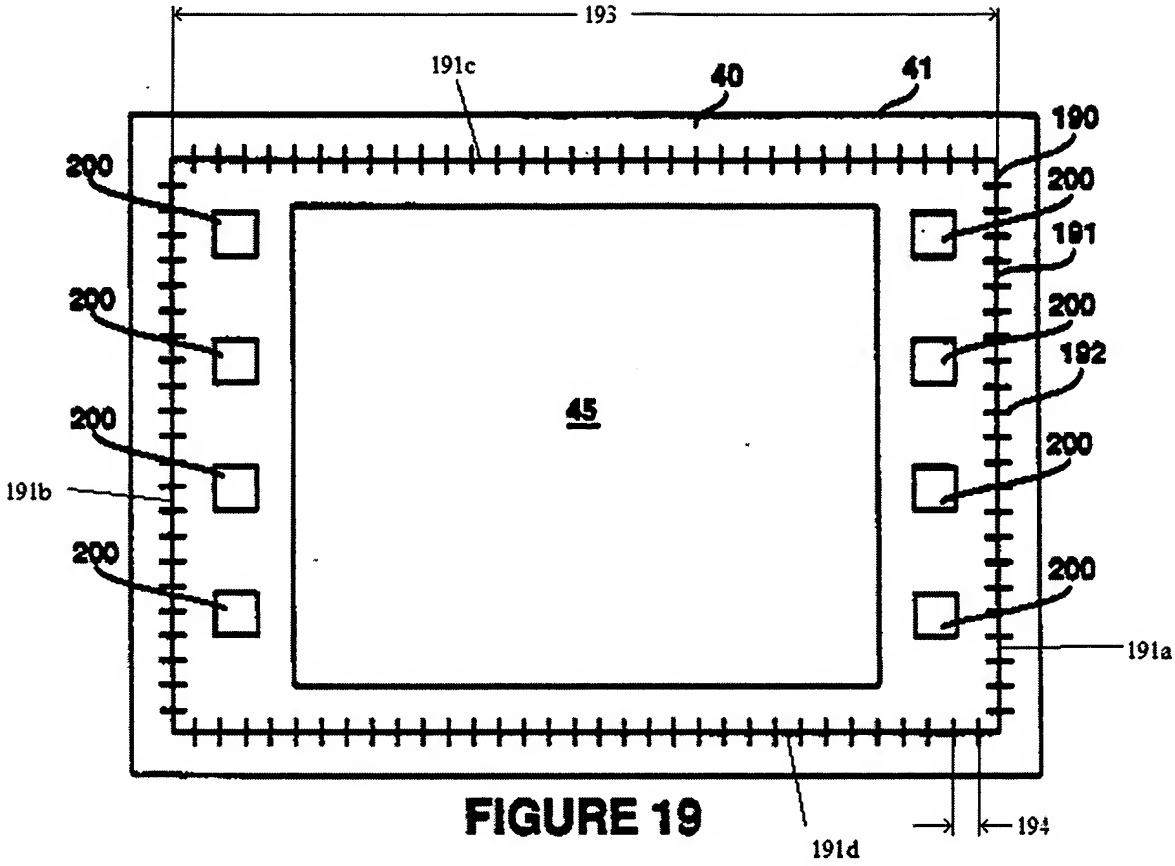


FIGURE 19

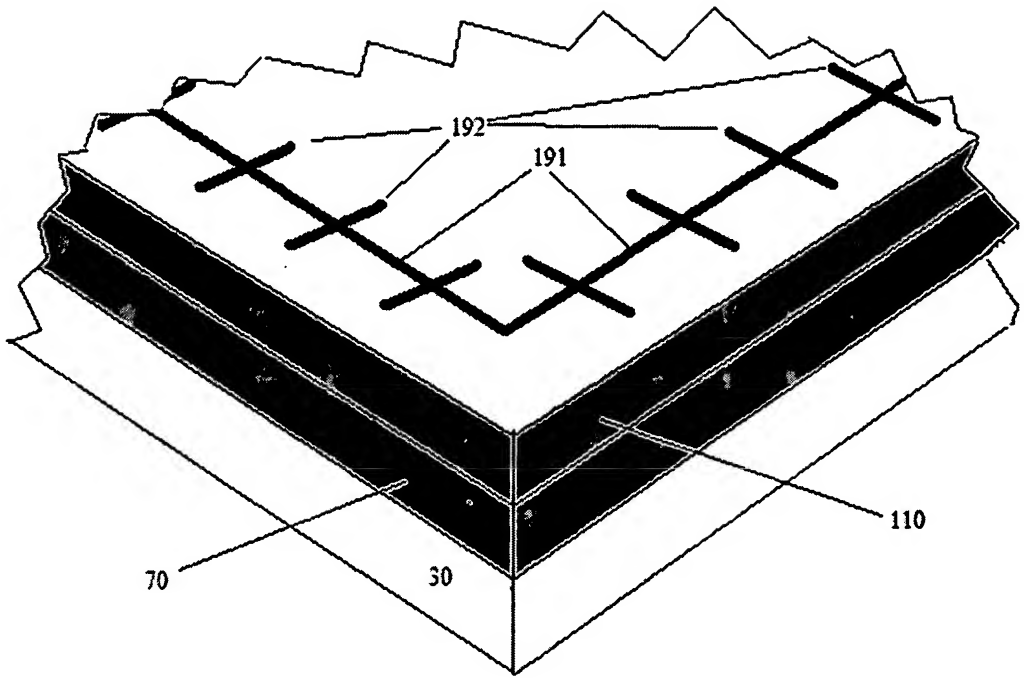


Figure 1

Regarding claim 2, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 1, wherein said third (Dinkel et al., Fig. 3A (34, 36)) groove portion is formed between said first (Dinkel et al., Fig. 3A (30))(Bost et al., Fig. 19 (191)) groove portion and said second (Dinkel et al., Fig. 3A (32)) groove portion.

Regarding claim 3, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 1, wherein said third (Dinkel et al., Fig. 3A (34, 36)) groove portion links said first (Dinkel et al., Fig. 3A (30)) (Bost et al., Fig. 19 (191)) groove portion and said second (Dinkel et al., Fig. 3A (32)) groove portion.

Regarding claim 4, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 1, wherein said first (Dinkel et al., Fig. 3A (30)) (Bost et al., Fig. 19 (191)), second (Dinkel et al., Fig. 3A (32)) and third (Dinkel et al., Fig. 3A (34, 36)) groove portions reach said main surface (upper surface of substrate (not shown in Dinkel et al.))(Bost et al., Fig. 18 and 19 (30a, 170)) from said top surface (Bost et al., Fig. 18 and 19 (110a)). Dinkel et al. discloses that to maximize the function of the device the crack stop (strip-like groove portions) should be formed in every layer of the device (Dinkel et al., Col. 3, Lines 8-10).

Regarding claim 5, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 1, wherein said first (Dinkel et al., Fig. 3A (30)) (Bost et al., Fig. 19 (191)) and second (Dinkel et al., Fig. 3A (32)) groove portions are formed along said peripheral edge (Bost et al. (edges of insulating layer 70 and 110))(the edges of 70 and 110 can be seen more clearly in gray in Figure 1 (drawn by the examiner), above) to surround a region (Bost et al., Fig. 19 (45)) where said semiconductor element (Bost et al., Fig. 19 (located within region (45))) (Bost et al., Col 5, Lines 5-8) is formed (Dinkel et al., Col. 2, Lines 25-36).

Regarding claim 6, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 1, wherein said interlayer insulating film (Bost et al., Figs. 18 and 19 (70,110)) includes first (70) and second (110) portions of different types (Oxide and

BPSG)(Bost et al., Col 5, Lines 12-15, 45-47) from each other and successively formed on said main surface (see Fig. 8-10 of Bost, et al).

Regarding claim 7, Bost et al. and Dinkel et al. disclose a semiconductor device comprising:

a semiconductor substrate (Bost et al., Fig. 18 (30)) having a main surface (Bost et al., Fig. 18 (30a, 170));

a semiconductor element (Bost et al., Fig. 19 (located within region 45)) (Bost et al., Col 5, Lines 5-8)) formed on said main surface (Bost et al., Fig. 18 (30a, 170)) and having side surfaces (Bost et al., Fig. 19 (defined by the edges of rectangle defining semiconductor element region (45)))(Dinkel et al., Fig. 1 (side surfaces of active area (18)))(Dinkel et al., Col. 2, Lines 25-36);

an interlayer insulating film (Bost et al., Fig. 18 (70,110)) having a top surface (Bost et al., Fig. 18 (110a)) and a peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), above) extending from said top surface (Bost et al., Fig. 18 (110a)) to said main surface (Bost et al., Fig. 18 (30a, 170)), and formed on said main surface (Bost et al., Fig. 18 (30a, 170)) to cover (Bost et al., Col.5, Lines 12-15) (Dinkel et al., Col. 2, Lines 25-36) said semiconductor element (Bost et al., Fig. 19 (located within region 45)) (Bost et al., Col 5, Lines 5-8)), wherein in said interlayer insulating film (Bost et al., Fig. 18 (70,110)), strip-like first (Dinkel et al., Fig. 3B (38)) and second (Dinkel et al., Fig. 3B (39)) groove portions are formed to be placed between a first side surface of

said semiconductor element (Bost et al., Fig. 19 (one edge of rectangle defining semiconductor element region (45))) (Bost et al., Col 5, Lines 5-8)) (Dinkel et al., Fig. 1 (side surface of active area (18)))(Dinkel et al., Col. 2, Lines 25-36) and said peripheral edge (the edges of 70 and 110 as seen in gray in Figure 1 (drawn by the examiner), above), to extend in parallel with said main surface (Bost et al., Fig. 18 (30a, 170)) and to extend to cross each other at predetermined spacing (In Fig. 3B of Dinkel et al. it can be seen that groove portions 38 and 39 cross each other at a spacing).

a metal filling said first and second groove portions (Dinkel et al., Col. 2, Lines 40-44), wherein said first and second groove portions contiguously extend along the first side surface of said semiconductor element (Dinkel et al., Fig. 1 (first and second groove portions (12, 14) can be seen extending along one side of active area (18))).

Regarding claim 8, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 7, wherein said first (Dinkel et al., Fig. 3A (30)) (Bost et al., Fig. 19 (191)) and second (Dinkel et al., Fig. 3A (32)) groove portions reach said main surface (upper surface of substrate (not shown in Dinkel et al.))(Bost et al., Fig. 18 and 19 (30a, 170)) from said top surface (Bost et al., Fig. 18 and 19 (110a)). Dinkel et al. discloses that to maximize the function of the device the crack stop (strip-like groove portions) should be formed in every layer of the device (Dinkel et al., Col. 3, Lines 8-10).

Regarding claim 9, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 7, wherein said first (Dinkel et al., Fig. 3A (30)) (Bost et al., Fig. 19 (191)) and second (Dinkel et al., Fig. 3A (32)) groove portions are formed along said peripheral edge (Bost et al. (edges of insulating layer 70 and 110))(the edges of 70 and 110 can be seen more clearly in gray in Figure 1 (drawn by the examiner), above) to surround a region (Bost et al., Fig. 19 (45)) where said semiconductor element (Bost et al., Fig. 19 (located within region (45))) (Bost et al., Col 5, Lines 5-8) is formed (Dinkel et al., Col. 2, Lines 25-36).

Regarding claim 10, Bost et al. and Dinkel et al. disclose the semiconductor device of claim 7, wherein said interlayer insulating film (Bost et al., Figs. 18 and 19 (70,110)) includes first (70) and second (110) portions of different types (Oxide and BPSG)(Bost et al., Col 5, Lines 12-15, 45-47) from each other and successively formed on said main surface (see Fig. 8-10 of Bost, et al).

### *Response to Arguments*

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Seshan et al. (U.S. Patent # 6137155), Agarwala et al. (U.S. Patent # 6734090), Davis et al. (U.S. Patent # 6650010), Toyoda (U.S. Patent # 6605861), and Ma et al. (U.S. Patent # 6509622) all disclose similar semiconductor devices.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFK

GEORGE ECKERT
PRIMARY EXAMINER